THAT WHICH IS CLAIMED IS:

1. A bipolar structure comprising:

a silicon carbide substrate;

a voltage blocking region on said substrate;

respective p-type and n-type silicon carbide regions bounding said voltage blocking region; wherein at least one of said p-type region and said n-type region has a thickness greater than the minority carrier diffusion length in that region.

2. A bipolar structure according to Claim 1 wherein said substrate, said voltage blocking region and said p-type and n-type regions all have the same polytype.

3. A bipolar structure according to Claim 2 wherein said substrate has a polytype selected from the group consisting of the 3C, 4H, 6H and 15R polytype of silicon carbide.

4. A bipolar structure according to Claim 1 wherein said bipolar structure forms a portion of a device selected from the group consisting of p-n junction diodes, p-i-n diodes, bipolar transistors, and thyristors.

5. A bipolar structure according to Claim 1 further comprising at least one stacking fault, and wherein those portions of those stacking faults that grow under forward bias operation are segregated from at least one of the interfaces between the p-type region or the n-type region and a portion of the device structure other than the voltage blocking region.

6. A bipolar structure according to Claim 1 further comprising at least one stacking fault, and wherein said stacking fault is segregated from any portion of the device that has a sufficient defect density or stress state to support the growth of the stacking fault under forward bias operation of the device.

7. A p-n diode comprising:

a silicon carbide substrate;

an n+ region of silicon carbide on said substrate;

an n- voltage blocking region of silicon carbide on said n+ region;

a p region of silicon carbide on said n- region;

wherein at least one of said p region and said n+ region has a thickness greater than the minority carrier diffusion length in said region.

8. A p-n diode according to Claim 7 wherein said substrate, said voltage blocking region and said p-type and n-type regions all have the same polytype.

9. A p -n diode according to Claim 8 wherein said substrate has a polytype selected from the group consisting of the 3C, 4H, 6H and 15R polytypes of silicon carbide.

10. A p -n diode according to Claim 7 wherein said n+ region is about 2.5 microns thick and has a carrier concentration of between about 1×10^{18} and 1×10^{19} cm^{-3}.

11. A p -n diode according to Claim 7 wherein said n+ region is about 0.5 microns thick and has a carrier concentration of about 2×10^{18} cm^{-3}.

12. A p -n diode according to Claim 7 wherein said p-type region is greater than about 0.5 microns thick and has a carrier concentration of between about 1×10^{17} and 1×10^{19} cm^{-3}.

13. A p- n diode according to Claim 7 wherein said p-type region includes a contact layer having a thickness of about 2 microns and a carrier concentration of about 1×10^{19} cm^{-3}.

14. A p- n diode according to Claim 7 wherein said p-type region has a carrier concentration about 2 orders of magnitude greater than said n- region.

15. A p- n diode according to Claim 7 and further comprising a p-type contact layer between said ohmic contact and said p-type region, with said contact layer having a higher carrier concentration than said p-type region.

16. A p- n diode according to Claim 15 wherein said contact layer has a carrier concentration of at least about 1 x 1019 cm-3, but less than the amount that would result in a decrease in crystal quality that would degrade the performance of the diode, and a thickness of at least about 1000 angstroms.

17. A p- n diode according to Claim 7 wherein said substrate has a carrier concentration of between about 5×10^{18} and 2×10^{19} cm^{-3} and is at least about 125 microns thick.

18. A p- n diode according to Claim 7 wherein:

said p-type region is about 0.5 microns thick and has a carrier concentration of about 1×10^{18} cm^{-3};

said n- region is about 45 microns thick and has a carrier concentration of about 1×10^{15} cm^{-3};

said n+ region is about 0.5 microns thick and has a carrier concentration of about 2×10^{18} cm^{-3};

and further comprising a p+ -type contact layer between said p-type region and said ohmic contact, said contact layer being about 2 microns thick and having a carrier concentration of about 1×10^{19} cm^{-3}.

and further comprising a n+ -type boundary layer between said n-type region and said substrate, said boundary layer being about 2 microns thick and having a carrier concentration of about 1×10^{19} cm^{-3}.

19. A p-n diode according to Claim 7 further comprising at least one planar defect, and wherein those portions of those stacking faults that grow under forward bias operation

are segregated from at least one of the interfaces between the n+ region or the p-type region and the remainder of the device.

20. A p- n diode according to Claim 7 further comprising at least one planar defect, and wherein said planar defect is segregated from any portion of the device that has a sufficient defect density or stress state to support the growth of the stacking fault under forward bias operation of the device.

21. A bipolar device comprising:

a silicon carbide substrate;

a voltage blocking region on said substrate;

respective p-type and n-type silicon carbide regions bounding said voltage blocking region; wherein those portions of those stacking faults that grow under forward bias operation are segregated from at least one of the interfaces between the bounding regions and the remainder of the device.

22. A bipolar device according to Claim 21 selected from the group consisting of p-i-n diodes, p-n junction diodes, bipolar transistors, and thyristors.

23. A bipolar device according to Claim 21 wherein said p and n regions have the same polytype.

25. A bipolar device according to Claim 24 wherein said substrate and said p and n regions have the same polytype.

26. A bipolar device according to Claim 25 wherein said polytype is selected from the group consisting of the 3C, 4H, 6H and 15R polytypes of silicon carbide.

27. A bipolar device according to Claim 21 wherein those portions of those stacking faults that grow under forward bias operation are segregated from the interfaces between the bounding regions and the remainder of the device.

28. A bipolar device according to Claim 4 wherein at least one of said p-type region and said n-type region has a thickness greater than the minority carrier diffusion length in that layer.

29. A bipolar device comprising:

at least one p-type region;

at least one n-type region; and

at least one stacking fault;

said stacking fault being segregated from any portion of the device that has a sufficient defect density or stress state to support the growth of the stacking fault under forward bias operation of the device.

30. A bipolar device according to Claim 29 selected from the group consisting of p-i-n diodes, p-n junction diodes, bipolar transistors, and thyristors.

31. A bipolar device according to Claim 29 wherein said p and n regions have the same polytype.

32. A bipolar device according to Claim 29 and further comprising a silicon carbide substrate.

33. A bipolar device according to Claim 32 wherein said substrate and said p and n regions have the same polytype.

34. A bipolar device according to Claim 33 wherein said polytype is selected from the group consisting of the 3C, 4H, 6H and 15R polytypes of silicon carbide.

35. A bipolar device according to Claim 29,

further comprising an active region including said p-type region and said n-type region, said p-type region and said n-type region forming boundary regions of said active region; and

wherein those portions of those stacking faults that grow under forward bias operation are segregated from the interfaces between the active region and the remainder of the device.

36. A bipolar device according to Claim 29 wherein said p-type layer and said n-type layer each have a thickness greater than the minority carrier diffusion length in that layer.

37. A bipolar device in silicon carbide wherein the thickness of any terminating layer is greater than the minority carrier diffusion length in that layer.

38. A bipolar device according to Claim 37 wherein said terminating layers comprise an epitaxial layer adjacent a substrate and an epitaxial layer adjacent an ohmic contact.

39. A bipolar device according to Claim 38 wherein said terminating layers comprise at least one n-type layer and at least one p-type layer, and wherein said epitaxial layers and said substrate all have the same polytype.

40. A bipolar device according to Claim 37 wherein said polytype is selected from the group consisting of the 3C, 4H, 6H, and 15R polytypes of silicon carbide.

41. A bipolar device according to Claim 37 selected from the group consisting of p-n junction diodes, p-i-n diodes; bipolar transistors, and thyristors.

42. A bipolar device according to Claim 37 that includes at least one stacking fault and wherein those portions of those stacking faults that grow under forward bias operation

are segregated from at least one of the interfaces between the active region and the remainder of the device.

43. A bipolar device according to Claim 37 that includes at least one stacking fault and wherein said stacking fault is segregated from any portion of the device that has a sufficient defect density or stress state to support the growth of the stacking fault under forward operation of the device.

44. A bipolar device formed in silicon carbide and within which continued growth of stacking faults is hindered by providing at least one highly doped layer in which an edge of a stacking fault will tend to terminate.

45 A bipolar device according to Claim 44 that includes a stacking fault having an edge that terminates in a layer having a carrier concentration of at least about 5E18 cm^{-3}.

46. A bipolar junction transistor comprising:

a silicon carbide substrate;

an n+ buffer layer on said substrate;

an n- region on said buffer layer;

a p-type base region adjacent said n- region;

an n+ emitter region adjacent said base region;

an ohmic contact deposited on said emitter region;

wherein at least one of said emitter region and said buffer layer has a thickness greater than the minority carrier diffusion length in that layer.

47. A thyristor comprising:

a silicon carbide substrate;

an n+ buffer layer on said substrate;

a p- region on said buffer layer;

an n-type region adjacent said p- region;

a p+ anode region adjacent said n-type region;

an ohmic contact deposited on said anode region;

wherein at least one of said anode region and said buffer layer has a thickness greater than the minority carrier diffusion length in that layer.

48. A field controlled thyristor comprising:

a silicon carbide substrate;

an n+ buffer layer on said substrate;

a p- drift region on said buffer layer;

a p+ anode region on said p- drift region; and

an ohmic contact deposited on said anode region;

wherein at least one of said anode region and said buffer layer has a thickness greater than the minority carrier diffusion length in that layer.

49. A p-n diode according to Claim 10 wherein said n+ region comprises a first n+ region having a thickness of about 0.5 microns and a carrier concentration of about 2E18 cm^{-3} and a second n+ region having a thickness of about 2.0 microns and a carrier concentration of about 1E19 cm^{-3}.

50. A p-n diode according to Claim 10 wherein said n+ region has a thickness of about 2.5 microns and a carrier concentration of about 2E18 cm^{-3}.

51. A p-n diode according to claim 20, wherein the planar defect is a stacking fault.